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Design and Simulation of a Linear Amplifier in C Band

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***Abstract*: -**Though there exists a variety of amplifier specifications for various purposes, most of the amplifiers are designed to work in a lower frequency band, and those that work in higher frequencies are optimized for higher efficiency and not for linearity. This paper describes the approach to design and simulate a Class A small signal Linear Amplifier that works in C Band. The bias network, matching network and the cascaded amplifier stages of the system are designed and simulated. The simulation yields the values of the S parameters and the resulting gain. The system is expected to provide a gain of 30dB and work in a frequency range of 5-6 GHz of the C band.

***Index Terms*: -** C Band, Linear Amplifier, S parameters

I. INTRODUCTION

One of the most basic concepts in microwave circuit design is amplification. In the past microwave tubes and microwave diodes (based in negative resistance region) were commonly used; However, nowadays use of microwave transistors (BJT or FET) has become very popular.

Transistor amplifiers are built rugged and are reliable for low power to medium power applications. We consider the design of linear small-signal pre-amplifier which works in C band. The design method used is based on the S parameters of the transistor, which forms the heart of the amplifier circuit.

An amplifier is used to increase the amplitude of a signal waveform, without changing other parameters of the waveform such as frequency or wave shape. They are one of the most commonly used circuits in electronics and perform a variety of functions in a great many electronic systems.

Radio Frequency amplifiers are tuned in which the frequency of operation is governed by a tuned circuit. This circuit may or may not, be adjustable depending on the purpose of the amplifier. Bandwidth also depends on use and may be relatively wide, or narrow. Input resistance is generally low, as is gain. (Some RF amplifiers have little or no gain at all but are primarily a buffer between a receiving antenna and later circuitry to prevent any high level unwanted signals from the receiver circuits reaching the antenna, where it could be re-transmitted as interference). A special feature of RF amplifiers where they are used in the earliest stages of a receiver is low noise performance. It is important that background noise generally produced by any electronic device, is kept to a minimum because the amplifier will be handling very low amplitude signals from the antenna (μV or smaller). For this reason it is common to see low noise FET transistors used in these stages.

II. RELATED WORK

RF Amplifiers are widely used analog building blocks in most electronic circuits. Some of the existing designs studied include the design, simulation and fabrication process.

RF amplifiers function very differently from other amplifiers. In a large-signal power amplifier, nonlinear effects are very strong because transistor parameters depend on many factors. In this research the authors have designed two stage microwave power amplifier having the operation frequency 2.4 GHz ISM Band to achieve the gain of +10~12dB and output power of 0.5 Watt (27dBm) within the size of 2.5x2.5 inch. They chose to work with ATF50189, which is a packaged AlGaAs/InGaAs FET [1].

A discrete 2-stage L-band low noise amplifier is designed. The amplifier is centred at 1.25 GHz with a noise figure (NF) less than 0.17 dB over a band width of 200 MHz.GaAs HEMT's offer low noise figure compared to MESFET's and silicon FET's. So, Agilent HEMT's are used in the 1st and 2nd stage respectively to obtain a overall noise figure less than 0.17 dB and gain more than 22dB. Amplifier is designed using ADS[2].

A three-stage monolithic microwave integrated circuit (MMIC) power amplifier from 6–18 GHz, which achieves high output power with excellent efficiency, is designed, fabricated and tested. Measured results show that the saturated output power and the small signal gain are about 32 dB and 23 dB, respectively. Thus, the power added efficiency of about 28% indicates that it is useful in various communication systems [3].

A 13.5GHz CMOS wideband amplifier is proposed with high power efficiency to achieve a high-speed D-band wireless receiver. From measurement, the peak gain is 25dB with the power consumption was 140mW with a supply voltage of 1.1V. As a result, the performance characteristics required to realize a low-power front-end amplifier for a D-band wireless receiver were obtained[4].

It is concluded that most of the amplifiers are designed to work at lower frequencies and those that work at

higher frequencies are generally optimized for efficiency and power gain and not linearity. The most obvious and simple way to ensure a high degree of linearity at higher frequencies is to design a class A small signal transistor amplifier.

III. DESIGN

The amplifier to be designed is a pre-amplifier with pre-defined specification. The design procedure involves the selection of a transistor, construction of the input and output matching networks, designing of the cascaded stages and verification of the design by testing various parameters of the transistor. The design process uses S parameters to characterize the transistor.

A. The Simulation Tool

The software design tool chosen for simulation is Agilent Technologies'Advanced Design System [5]. ADS provides a vast array of simulation modes and models. For design of high speed digital circuits, the most useful simulation tools will be DC and transient analysis. Whether to use ADS or HSPICE is a matter of individual preference. Since ADS is oriented toward microwave applications, it is found that it contains a much larger library of transmission line and passive component models that include non idealities of these components. When dealing with high speed interconnections, this might provide the incentive to learn to use ADS over HSPICE user. On the other hand, ADS has yet to handle transistor model libraries in a convenient manner.

B. The Transistor

We have chosen for the design is FLC057WG. The FLC057WG is a power GaAs FET that is designed for general purpose applications in the C-band frequency range as it provides superior power, gain, and efficiency.
The range of frequencies that form the operating range of the amplifier is 5-6 GHz, which is the working frequency range of the chosen transistor. The Id-Vds characteristics of the transistor are observed and for the purpose of biasing the middle of the active region is chosen so that the characteristic of the amplifier are linear. The middle of the active region corresponds to voltage levels of Vgs=-1 V and Vds= 5 V. The bias levels are added to the circuit to complete the design.
The datasheet of the chosen transistor is downloaded to get information about the transistor. The datasheet of the transistor briefly lists down the features, description, Voltage Power and Temperature ratings, along with the electrical characteristics. The current vs voltage characteristics are also a part of the datasheet. The transistor libraries are available for download in ADS.

C. The Design Procedure

The first step is to design an input and output matching circuit. The transistor is attached to terminal loads on the input and output side as shown in the figure. The S parameter simulation icon is inserted into the schematic. This is the basic way to start the design to find out the S parameters of the device. The circuit consists of an FET working between (0.10-10.00 GHz) and two terminal loads attached on either ends. Once the above circuit is simulated the S parameters (dB) and the smith chart is plotted. Markers are placed at the required 5 GHz point. The corresponding S_{11} and S_{22} are observed. The impedance value of $Z_o$for S_{11} is calculated and will be used. Then a Smith Chart Utility is created. Keeping the source impendence Z_{s*} constant (corresponding to the terminal load) and changing $Z_{L.}$ to correspond to the transistor, we get two points on the impedance and admittance circle of the smith chart. We use the admittance or the impedance circles to match the two points till we get a suitable network response and note down the circuit appearing on the Network Schematic. Construct the input matching circuit from the Network Schematic. A combination of Series L and Shunt C is used Note down values of the capacitor and inductor and Simulate. Simulated results of input matching are obtained and we get a gain > -10dB on the db vs frequency plot. The gain is insufficient and the matching is inefficient. The circuit is shown in Figure 1.

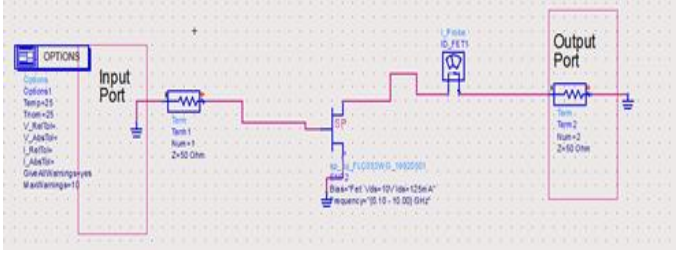

Fig. 1. Transistor with input and output matching circuits

Therefore, to increase the gain, the gate thickness must be increased by cascading amplifiers. The design procedure from the design of the input and output matching circuits is repeated for the new transistor stage

consisting of 2 FETs. A bias network is then with Vgs=-1 V and V_{ds}=5V. These values are obtained from the datasheet of the transistor. Since we are biasing our transistor is linear and thus a corresponding value is checked in the active region. The forward gain obtained is around 20 dB. The obtained design and simulation results are shown in Figure 2 and Figure 3. The circuit shows better stability and matching that the circuit simulated earlier.

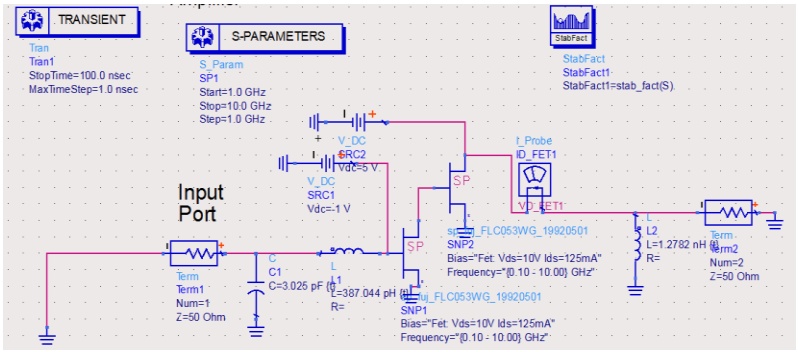

Fig. 2. Schematic with biasing circuit

The stability factor (K) is also measured and plotted 'K' for the simulated circuit using the software. 'StabFact' is added to the schematic in order to plot the stability factor. This would help in quantitatively determining how stable the circuit is at the mentioned frequency. The transient response of the system is observed and verified by plotting the transient current and voltage across the device.Finally the noise figure of the circuit is plotted and its variation with respect to frequency is analyzed. For this purpose a noise source is added at the input terminal and the circuit is simulated.

IV. RESULTS

The simulation yields the values of the S parameters and with a two stage amplifier we obtain the gain as 19.241 dB

S_{11}= -19.662dB = 0.104∠165.568
S_{22}= -19.478dB = 0.004∠139.658
S_{12}= 48.157dB = 9.163∠ -136.342
S_{21}= 19.241dB = 0.106∠ -48.86
Stability factor=13.673
These are shown in Figure 3.

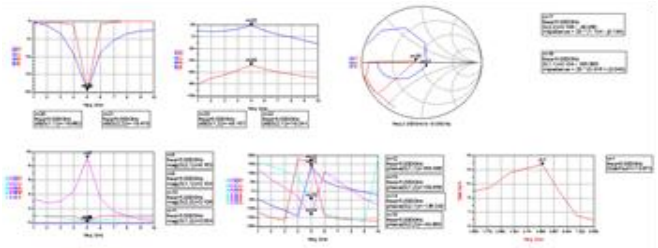

Figure 3: Results of simulation

The plot for stability factor shows that the stability peaks at the given frequency of 5GHz. The transient response as shown in Figure 4 shows the linear characteristic of the transistor as well as the amplification generated by the circuit. The noise analysis shows the noise figure around 3 dB, which is as expected is a low noise pre-amplifier. The plot obtained is shown in Figure 5.

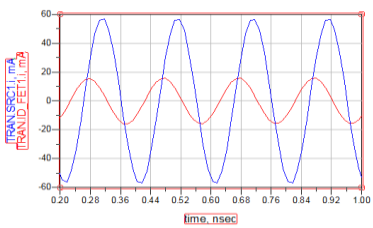

Fig. 4. Results of transient simulation

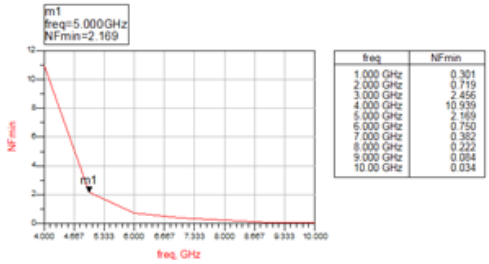

Fig. 5. Result of noise analysis.

V. CONCLUSION

In this work our focus was to obtain a gain of 30dB, a noise figure of less than 3dB, a stability factor of greater than 1 and to compare it with the simulated results. The gain can be increased by cascading multiple staged with suitable matching circuits. The noise figure was obtained to be around 3dB. The stability factors indicate that the circuit is stable within the said frequency range.

The future scope of the project involves attempting to increase the forward gain by cascading amplifier stages. Fabrication of the simulated design and the subsequent testing also can be done.

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